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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,121	EVANS, PAUL	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 20* is/are allowed.

6)☒ Claim(s) *1-3,6-18,21 and 22* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7-8, 10, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 7-8, lines 2-3, it is confuse. Applicant recites, "the circuit components...signals, in claim 1, lines 5-6", and also, disclosed in claims 7-8 "the circuit components...signals, lines 2-3" does applicant mean "there are more, another, or different a transport stream generating device?"

Regarding claims 10 and 17, it is confuse. Does applicant mean "a device, line 2" different from "a transport stream generating device" of claims 1 and claim 13?

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application

being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-3, 6-18, and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Khosrowpour et al. (U. S. Patent 6,477,593).

With respect to claims 1, and as best understood to claims 7-8, Khosrowpour discloses a stackable module (100, column 4, lines 9-10) as shown in figures 1-4 for a processor system comprising:

a support plate (120;130, column 4, line 12) having a topside and an underside;

a set of topside circuit component (see figures 1-2, each of boards 120 or 130 having a plurality of components, for example: IC chips and CPU (represent element 134 which are bus interfaces or I/O bridge circuits) mounted on each board) mounted on the topside of the support plate (120, 130), the circuit components (134-figure 3) constituting a transport stream generating device which generates transport stream data and transport stream control signals;

topside and underside connectors (board 120 having top connector (122A, 122B) and bottom connector (122C, 122D)) mounted to the topside and underside of the support plate; and

first and second set of conductive tracks (114A, 114B) connected directly between the topside and underside connectors and connecting the topside connector to the set of topside circuit components respectively; the topside and underside connectors being engageable with respective underside connector and topside

connector of other modules (for example board 130), the first and second conductive track arranged to convey transport stream data transport stream control signals between modules in a stack (column 2, lines 1-5, and column 3, lines 49-58).

With respect to claims 11, 13-15, and 18, Khosrowpour, see figures 1-4, discloses a stack of modules in a processor system, the stack comprising:

a main board (motherboard-110) having an interface connector (112A, 112B) and a set of main board components (see figure 1), the interface connector providing a set of pins for conveying transport stream data and transport stream control signals (see figure 3);

at least one module (daughter boards 120, 130) comprising a support plate having topside and underside, the topside having a set of circuit components (see figures 1-2), the support plate with topside and underside connectors (122A-122B, 122C-122D) mounted to topside and underside of the support plate respectively, the at least one module having the set of circuit components comprising a transport stream generating device configured to generate the transport stream data and the transport stream control signals (see columns 2-3), the underside connector (122C-122D) being connected to the interface connector (112A-112B) of the main board (110) for the conveying transport stream data and the transport stream control signals from the at least one module to the interface connector of the main board.

With respect to claim 12, Khosrowpour, see figures 1-4, discloses a stack of modules in a processor system, the stack comprising:

a main board (110) having an interface connector (112) and a set of main board components (see figure 1), the interface connector providing a set of pins;

at least one module (120, 130) comprising:

a support plate having a topside and an underside;

a set of topside circuit components (IC chips and CPU, for example: I/O bridge circuits or interface buses) mounted on the topside of the support plate and comprising a transport stream generating device configured to generate the transport stream data and the transport stream control signals (see columns 2-3); a topside connector mounted to the topside of the support plate; an underside connector (122C-122D) connected to the interface connector (112) of the main board (110);

first and second set of conductive tracks (114) connected directly between the topside connector and the underside connector and the topside connector to the topside circuit component, the underside connector and the topside connector being engaged with respective underside connectors and topside connectors of the other stack of modules, the first and second conductive tracks arranged to convey the transport stream data and the transport stream control signals between the stack of modules (see columns 2-3).

Regarding claims 21-22, Khosrowpour discloses the stackable module as shown in figures 1-4 comprising:

a support plate (boards 120, 130) having a topside and an underside;

a set of topside circuit components mounted on the topside of the support plate (120; 130) constituting a device to generate a transport stream data and transport stream control signals;

topside and underside connectors mounted to the topside and underside of the support plate, respectively;

first and second set of conductive tracks (114) connected directly between the topside connector and the underside connector and the topside connector to the topside circuit component, the underside connector and the topside connector being engaged with respective underside connectors and topside connectors of the other stack of modules, the first and second conductive tracks arranged to convey the transport stream data and the transport stream control signals between the stack of modules (see columns 2-3); and a multiplexor (the IC chips, memory, or CPU capable of being multiplexor).

Regarding claim 2, Khosrowpour, see figures 1-4, discloses each of the topside and underside connectors comprises a set of pins for carrying memory access signals to enable the module to function as an external memory interface.

Regarding claim 3, Khosrowpour, see figures 1-4, discloses the topside connector is a receptacle and the underside connector is a plug (see figure 3).

Regarding claim 6, Khosrowpour, see figures 1-2, discloses a connector space-defining component (flat chip) that extends from the support plate by a distance calculated to define the minimum spacing between modules in the stack.

As best understood to claims 9-10, 16-17, Khosrowpour, see figures 1-4, discloses the circuit components (IC chips, CPU, or elements 124, 134) capable of being multiplexor or device constitute a transport stream generating device that generate the transport stream data and the transport stream control signals.

Allowable Subject Matter

5. Claims 4-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 19-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Neither the references cited nor the cited references teach or suggest a stackable printed circuit board (PCB) configured for stacking on a motherboard and with other stackable printed circuit boards (PCBs) in combination comprising: at least one support pillar extending from a top surface of a PCB; and at least one through hole formed in the PCB and adapted to receive a support pillar from another stackable PCB.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant's arguments filed 05/21/03 have been fully considered but they are not persuasive.

Applicant argues:

Khosrowpour does not disclose "the circuit components constituting a transport stream generating device which generates transport stream data and transport stream control signals"

Examiner disagrees.

Khosrowpour clearly discloses in figures 1-4 that the daughter boards (120, 130) having a plurality of components (i.e. IC chips memory, and CPU) mounted on. One of the components can represent as the I/O bridge circuits (134) or interface buses. Each of the I/O bridge circuits (interface buses-134) has functions as received/transmitted data and signals between each of the interface buses and providing information convey to the motherboard. Thus the components generate the transport stream data and transport stream control signals (see column 2, lines 1-5, and column 3, lines 49-58).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kranzler et al. and Dell et al. disclose related art.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
August 08, 2003.

HAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800